1   CLAIMS

2   What is claimed is:

1   1.   A method comprising:

2   determining an optimum splitting variable;

3   dividing a set of equations representing a programmable logic array

4   (PLA) into a first set of equations representing a first sub-PLA and a second set

5   of equations representing a second sub-PLA based on the splitting variable;

6   determining a topological circuit representation of the equations

7   representing the first sub-PLA and the second sub-PLA;

8   applying gating logic to the topological circuit representation of the

9   equations representing the first sub-PLA and the equations representing the

10   second sub-PLA; and

11   controlling power consumption in the topological circuit

12   representation of the equations representing the first sub-PLA and the

13   equations representing the second sub-PLA so only one of the topological

14   circuit representation of the first sub-PLA and the second sub-PLA contributes

15   to power consumption.

1   2.   The method of claim 1, wherein the PLA to be divided is partially

2   optimized by computer aided design.

1   3.   The method of claim 1, further comprising merging an output of the

2   equations representing the first sub-PLA with an output of the equations

3   representing the second sub-PLA, wherein merging the output of the

4   equations representing the first sub-PLA with the equations representing the

5   second sub-PLA forms a logical equivalent of the PLA

1   4.   The method of claim 1, wherein an OR plane of the topological circuit

2   representation of the first sub-PLA is interleaved with an OR plane of the

3   topological circuit representation of the second sub-PLA.

1   5.   The method of claim 1, wherein an OR plane of the topological circuit

2   representation of the first sub-PLA is separated from an OR plane of the

3   topological circuit representation of the second sub-PLA.

1   6.   The method of claim 1, wherein the equations representing the first

2   sub-PLA includes a plurality of products where the splitting variable is

3   complemented and the equations representing the second sub-PLA includes a

4   plurality of products where the splitting variable is uncomplemented.

1   7.   The method of claim 1, further comprising delaying a clock to an OR

2   plane of one of the topological circuit representation of the first sub-PLA and

3   the topological circuit representation of the second sub-PLA.

1   8.   The method of claim 1, wherein the step of determining the optimum

2   splitting variable further comprises avoiding unbalanced columns in an AND

3   plane of the set of equations representing the PLA; and selecting a column

4   with smallest overhead in the AND plane of the set of equations representing

5   the PLA.

1   9.   The method of claim 1, wherein determining a topological circuit

2   representation of first sub-PLA and the second sub-PLA is created by computer

3   aided design.

1   10.   A method comprising:

2   determining an optimum splitting variable for dividing a set of

3   equations representing a programmable logic array (PLA);

4   dividing the set of equations representing the PLA into equations

5   representing a plurality of sub-PLAs ;

6   merging outputs of the equations representing the plurality of sub-

7   PLAs;

8   determining a topological circuit representation of the equations

9   representing the plurality of sub-PLAs;

10   applying gating logic to the topological circuit representation of the

11   plurality of sub-PLAs; and

12   controlling power consumption in the topological representation of the

13   plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes to

14   power consumption.

1   11.   The method of claim 10, wherein the PLA to be divided is partially

2   optimized by computer aided design.

1   12.   The method of claim 10, wherein the equations representing the

2   plurality of sub-PLAs are divided recursively based on a determined optimum

3   splitting variable for each equation representing a sub-PLA.

1   13.   The method of claim 12, wherein each product of the equations

2   representing the plurality of sub-PLAs is obtained by omitting literals in the

3   equations representing the PLA.

1   14.   The method of claim 13, wherein a product of the omitted literals is

2   used in the topological circuit representation of the plurality of sub-PLAs to

3   gate a clock of each product of the plurality of sub-PLAs.

1   15.   The method of claim 10, wherein the step of determining the optimum

2   splitting variable further comprises avoiding unbalanced columns in an AND

3   plane of the equations representing the PLA; and

4   selecting a column with smallest overhead in the AND plane of the equations

5   representing the PLA.

1   16.   The method of claim 12, wherein the step of determining the optimum

2   splitting variable for each of the equations representing the sub-PLA further

3   comprises avoiding unbalanced columns in an AND plane of the equations

4   representing the sub-PLA; and selecting a column with smallest overhead in

5   the AND plane of the equations representing the sub-PLA.

1   17.   A program storage device readable by a machine comprising

2   instructions that cause the machine to:

3   determine an optimum splitting variable;

4   divide a set of equations representing a programmable logic array (PLA)

5   into a first set of equations representing a first sub-PLA and a second set of

6   equations representing a second sub-PLA based on the splitting variable;

7   determine a topological circuit representation of first sub-PLA and the

8   second sub-PLA;

9   apply gating logic to the topological circuit representation of the first

10   sub-PLA and the second sub-PLA; and

11   control power consumption in the topological circuit representation of

12   the first sub-PLA and the second sub-PLA so only one of the first sub-PLA and

13   the second sub-PLA contributes to power consumption.

1   18.   The program storage device of claim 17, wherein the PLA to be divided

2   is partially optimized by computer aided design.

1   19.   The program storage device of claim 17, further comprising

2   instructions that cause the machine to merge an output of the equations

3   representing the first sub-PLA with an output of the equations representing

4   the second sub-PLA,

5   wherein the instruction that causes the machine to merge the output of the

6   equations representing the first sub-PLA with the equations representing the

7   second sub-PLA, forms a logical equivalent of the equations representing the

8   PLA.

1   20.   The program storage device of claim 17, wherein the topological circuit

2   representation an OR plane of the first sub-PLA is interleaved with an OR

3   plane of the second sub-PLA.

1   21.   The program storage device of claim 17, wherein in the topological

2   circuit representation an OR plane of the first sub-PLA is separated from an

3   OR plane of the second sub-PLA.

1   22.   The program storage device of claim 17, wherein the equations

2   representing the first sub-PLA includes a plurality of products where the

3   splitting variable is complemented and the equations representing the second

4   sub-PLA includes a plurality of products where the splitting variable is

5   uncomplemented.

1   23.   The program storage device of claim 17, wherein the instructions that

2   cause the machine to determine the optimum splitting variable further

3   comprises avoiding unbalanced columns in an AND plane of the set of

4   equations representing the PLA; and selecting a column with smallest

5   overhead in the AND plane of the set of equations representing the PLA.

1   determine an optimum splitting variable for dividing a set of equations

2   representing a programmable logic array (PLA);

3   divide the set of equations representing the PLA into equations

4   representing a plurality of sub-PLAs ;

5   merge outputs of the equations representing the plurality of sub-PLAs;

6   determine a topological circuit representation of the equations

7   representing the plurality of sub-PLAs;

8   apply gating logic to the topological circuit representation of the

9   plurality of sub-PLAs; and

10   control power consumption in the topological circuit representation of

11   the plurality of sub-PLAs so only one of the plurality of sub-PLAs contributes

12   to power consumption.

1   25.   The program storage device of claim 24, wherein the PLA to be divided

2   is partially optimized by computer aided design.

1   26.   The program storage device of claim 24, wherein the instruction

2   causing the machine to divide the equations representing the plurality of sub-

3   PLAs divides recursively based on a determined optimum splitting variable

4   for each equation representing a sub-PLA.

1   27.   The program storage device of claim 24, wherein the instruction

2   causing the machine to determine the optimum splitting variable further

3   comprises avoiding unbalanced columns in an AND plane of the equations

5   selecting a column with smallest overhead in the AND plane of the equations

6   representing the PLA.

1   28.   The program storage device of claim 26, wherein the instruction

2   causing the machine to determine the optimum splitting variable for each of

3   the equations representing the sub-PLA further comprises avoiding

4   unbalanced columns in an AND plane of the equations representing the sub-

5   PLA; and selecting a column with smallest overhead in the AND plane of the

6   equations representing the sub-PLA.